Reliable ESD Protection Device and Method for Advanced Sub-micron CMOS Technologies

Advantages
- Free from gate reliability problems
- Tunable
- Reliable during extreme operating conditions
- Facilitates the ability of sub-micron CMOS technology to pass a high level of ESD current without latchup or damage

Invention
A tunable, gateless, versatile, space-efficient and reliable ESD protection device and method for a more robust implementation of ESD protection systems, in advanced sub-micron CMOS technologies [U.S. Patent 7,285,828]

Background
For many years, the semiconductor industry has employed complementary metal oxide semiconductor (CMOS) technology to manufacture reliable integrated circuits (IC) at low cost. This technology is continually evolving to include production of smaller and faster devices which can be used in very large scale integration (VLSI) systems. Some of the existing electrostatic discharge (ESD) protection schemes can be migrated and still be effective in the new CMOS technologies. However, there is no guarantee that previously developed ESD solutions will continue to perform reliably when they are scaled down or resized. Actually, some ESD models tend to become more sensitive in the new CMOS technologies. One effort to address this has been to let the ESD protection module occupy more space on the chip. Unfortunately, this does not guarantee improved performance. Another measure employed to overcome this limitation is the use of devices such as silicon controlled rectifiers (SCRs), in which the current-voltage shows voltage snapback during ESD. This facilitates the design of smaller ESD protection systems while reducing leakage current during normal operation. However, the trigger voltage is very high increasing the possibility for severe damage to the sub-micron core circuit before the protection device triggers. Low voltage SCRs are used to deal with this, but they have the disadvantage of very low holding voltages that cause latchup problems.

A more viable solution, is a high-holding low voltage SCR (HHLVTSCR) that includes a gate to increase the speed with which a device responds to an ESD event. Such systems allow tuning of the holding voltage over a wide range while maintaining a relatively low trigger voltage. Still, their effectiveness comes into question for sub-micron CMOS applications. Systems with floating gates have been developed to correct this problem but in such systems, the conduction characteristics are unpredictably modified by the gate conditions, thus leading to unreliability. UCF scientists have developed a device that can be fabricated in the sub-micron CMOS technology, is free from the gate reliability problems and is able to pass a high level of ESD current without latchup or damage.

Application
This technology is applicable in the semiconductor industry where CMOS/BiCMOS mixed signals are used. It is also suitable for mixed voltage interface peripherals such as transceivers circuits for high speed data communication, charge pump circuits, voltage regulators and DC-DC converters and power management circuits.

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Selected References


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